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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,094	08/29/2001	Kazunobu Kuwazawa	81751.0017	7672

26021 7590 09/12/2002

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
SEFER, AHMED N	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)
	09/943,094	KUWAZAWA, KAZUNOBU
	Examiner	Art Unit
	A. Sefer	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-19) in Paper No. 7 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

3. Claims 1, 2 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Kato US PG-Pub 2001/0033001.

Kato discloses in fig. 4 a semiconductor substrate 304 having a first conductive layer 311 formed from an impurity layer (as in claim 2) provided therein; an insulation layer 305 provided above the semiconductor substrate; a semiconductor layer 301 provided above the insulation layer; and a second conductive layer 303 provided above the semiconductor layer, and electrically connected to the first conductive layer.

As to claim 5, Kato discloses a connection hole for connecting the first

conductive layer to the second conductive layer, and wherein a contact layer is provided in the connection hole.

4. Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Chittipeddi et al. US Patent No. 6,384,452.

Chittipeddi et al disclose in figs. 1-11 a semiconductor substrate 110 having a first conductive 130 functioning as a wiring layer (as in claim 3) layer provided therein; an insulation layer 115 provided above the semiconductor substrate; a semiconductor layer 120 provided above the insulation layer; and a second conductive layer 180 provided above the semiconductor layer, and electrically connected to the first conductive layer.

As to claim 4, Chittipeddi et al disclose a conductive layer 210 which functions as a resistance layer.

5. Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Igel et al. US Patent No. 5,933,715.

Igel et al disclose in figs. 1-3 a semiconductor substrate 13 having a first conductive 19 layer formed from an impurity (as in claim 2) provided therein; an insulation layer 12 provided above the semiconductor substrate; a semiconductor layer 10 provided above the insulation layer; and a second conductive layer 21 provided above the semiconductor layer, and electrically connected to the first conductive layer.

As to claim 5, Igel et al disclose a connection hole 16 for connecting the first conductive layer to the second conductive layer, and wherein a contact layer 20 is provided in the connection hole.

As to claim 6, Igel et al disclose a sidewall 17 provided in the connection hole.

6. Claims 7-9 and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Kato US PG-Pub 2001/0033001.

Kato discloses in fig. 4 semiconductor device comprising a semiconductor substrate or p-type substrate (as in claim 11) having a contact region 311 formed from an impurity layer (as in claim 8) or n-type contact region (as in claim 11) provided therein; an insulation layer 305 provided above the semiconductor substrate; and a semiconductor layer 306 provided above the insulation layer; and a conductive layer 303a provided above the semiconductor layer, and has a function of allowing charge to flow into the semiconductor substrate, said contact region being electrically connected to said conductive layer.

As to claim 9, Kato discloses a pn junction formed by the contact region and the semiconductor substrate.

As to claims 12 and 13, Kato discloses a connection hole having a sidewall (as in claim 13) for connecting the first conductive layer to the second conductive layer, and wherein a contact layer is provided in the connection hole.

7. Claims 7-9, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Igel et al. US Patent No. 5,933,715.

Igel et al disclose in figs. 1-3 semiconductor device comprising a semiconductor substrate 13 having a contact region 19 formed from an impurity layer (as in claim 8) provided therein; an insulation layer 12 provided above the semiconductor substrate; and a semiconductor layer 10 provided above the insulation layer; and a conductive

layer 21 provided above the semiconductor layer, and has a function of allowing charge to flow into the semiconductor substrate, said contact region being electrically connected to said conductive layer.

As to claim 9, Igel et al disclose a pn junction formed by the contact region and the semiconductor substrate.

As to claims 12 and 13, Igel et al disclose a connection hole 16 having a sidewall 17 (as in claim 13) for connecting the first conductive layer to the second conductive layer, and wherein a contact layer 20 is provided in the connection hole.

8. Claims 7-9 and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Davari et al. US Patent No. 6,188,122.

Davari et al disclose in figs. 1-7 semiconductor device comprising a semiconductor substrate or p-type substrate (as in claim 11) having a contact region 16 formed from an impurity layer (as in claim 8) or n-type contact region (as in claim 11) provided therein; an insulation layer 12 provided above the semiconductor substrate; and a semiconductor layer 14 provided above the insulation layer; and a conductive layer 30' provided above the semiconductor layer, and has a function of allowing charge to flow into the semiconductor substrate, said contact region being electrically connected to said conductive layer.

As to claim 9, Davari et al disclose a pn junction formed by the contact region and the semiconductor substrate.

As to claims 12 and 13, Davari et al disclose a connection hole having a sidewall (as in claim 13) for connecting the first conductive layer to the second conductive layer, and wherein a contact layer is provided in the connection hole.

9. Claims 7, 8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Witek US Patent No. 5,879,971.

Witek discloses (see figs. 1-3 and 22 and col. 2, lines 26-32) semiconductor device comprising a semiconductor substrate or n-type substrate (as in claim 10) having a contact region 82 formed from an impurity layer (as in claim 8) or p-type contact region (as in claim 10) provided therein; an insulation layer 84 provided above the semiconductor substrate; and a semiconductor layer 86 provided above the insulation layer; and a conductive layer 102 provided above the semiconductor layer, and has a function of allowing charge to flow into the semiconductor substrate, said contact region being electrically connected to said conductive layer.

10. Claims 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Witek.

Witek discloses in fig. 32 a semiconductor device comprising a semiconductor substrate having a first electrode 101 formed from a first impurity layer (as in claim 15) provided therein; an insulation layer 113 provided above the semiconductor substrate; a semiconductor layer 134 provided above the insulation layer, the semiconductor layer having a second electrode formed from a second impurity layer (as in claim 16) provided therein; and the first electrode, the second electrode, and the insulation layer in cooperation turning a capacitive element.

As to claim 17, Witek discloses a first electrode connected electrically to a conductive layer 140 provided above the semiconductor layer.

As to claims 18 and 19, Witek discloses a connection hole having a sidewall (as in claim 19) for connecting the first conductive layer to the second conductive layer, and wherein a contact layer is provided in the connection hole.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
September 5, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800